

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

- 1 1. A method for controlling data transfer between
2 embedded resources in a device using middleware,
3 comprising the steps of:
4 separating a functionality of said middleware
5 into a control interface and a data interface, said
6 middleware functionality enabling interoperability
7 of said device with other devices in a given
8 system, said other devices also using said
9 middleware to provide said functionality, said
10 middleware functionality also enabling a software
11 object resident on a general purpose processor of
12 said device to transfer data between said embedded
13 resources, there being a control interface and a
14 data interface for each of said object and each of
15 said embedded resources;
16 constructing said control interfaces within
17 said general purpose processor of said device;
18 extracting said data interfaces for said
19 embedded resources outside said general purpose
20 processor, such that said data transfer, under
21 control of said object exercised through said
22 middleware via said control interfaces, occurs
23 directly between said embedded resources without
24 going through said general purpose processor.
- 1 2. A method as in claim 1, wherein said respective
2 control interfaces for each of said embedded

3 resources are implemented using device drivers of
4 said respective embedded resources.

1 3. A method as in claim 1, wherein said respective
2 data interfaces for each of said embedded resources
3 are each connected to a switch matrix, said switch
4 matrix being external to said general purpose
5 processor and serving to connect said embedded
6 resources.

1 4. A method as in claim 3, wherein said switch
2 matrix is implemented as a connection fabric.

1 5. A method as in claim 3, wherein said switch
2 matrix is implemented as a shared memory.

1 6. A method as in claim 1, wherein said device is
2 a software defined radio, said given system is the
3 Joint Tactical Radio System, and said middleware is
4 compliant with Software Communications Architecture
5 (SCA).

1 7. A method as in claim 3, wherein one of said
2 embedded resources is a Field Programmable Gate
3 Array (FPGA).

1 8. A method as in claim 7, further comprising the
2 steps of:
3 creating an Interface Description Language
4 (IDL) description of a raw interface of said FPGA;
5 generating from said IDL a description of an
6 interface between a core functionality of said FPGA
7 and said switch matrix, and a description of a

8 controller for performing said core functionality;
9 and
10 integrating said core functionality interface
11 into said data interface of said FPGA, and
12 integrating said controller into said control
13 interface of said FPGA.

1 9. A system for controlling data transfer between
2 embedded resources in a device using middleware,
3 comprising:

4 means for separating a functionality of said
5 middleware into a control interface and a data
6 interface, said middleware functionality enabling
7 interoperability of said device with other devices
8 in a given system, said other devices also using
9 said middleware to provide said functionality, said
10 middleware functionality also enabling a software
11 object resident on a general purpose processor of
12 said device to transfer data between said embedded
13 resources, there being a control interface and a
14 data interface for each of said object and each of
15 said embedded resources;

16 means for constructing said control interfaces
17 within said general purpose processor of said
18 device;

19 means for extracting said data interfaces for
20 said embedded resources outside said general
21 purpose processor, such that said data transfer,
22 under control of said object exercised through said
23 middleware via said control interfaces, occurs
24 directly between said embedded resources without
25 going through said general purpose processor.

1 10. A system as in claim 9, wherein said
2 respective control interfaces for each of said
3 embedded resources are implemented using device
4 drivers of said respective embedded resources.

1 11. A system as in claim 9, wherein said
2 respective data interfaces for each of said
3 embedded resources are each connected to a switch
4 matrix, said switch matrix being external to said
5 general purpose processor and serving to connect
6 said embedded resources.

1 12. A system as in claim 11, wherein said switch
2 matrix is implemented as a connection fabric.

1 13. A system as in claim 11, wherein said switch
2 matrix is implemented as a shared memory.

1 14. A system as in claim 9, wherein said device is
2 a software defined radio, said given system is the
3 Joint Tactical Radio System, and said middleware is
4 compliant with Software Communications Architecture
5 (SCA).

1 15. A system as in claim 11, wherein one of said
2 embedded resources is a Field Programmable Gate
3 Array (FPGA).

1 16. A system as in claim 15, further comprising:
2 means for creating an Interface Description
3 Language (IDL) description of a raw interface of
4 said FPGA;

5 means for generating from said IDL a
6 description of an interface between a core
7 functionality of said FPGA and said switch matrix,
8 and a description of a controller for performing
9 said core functionality; and
10 means for integrating said core functionality
11 interface into said data interface of said FPGA,
12 and integrating said controller into said control
13 interface of said FPGA.